IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A multi-layer printed wiring board comprising:

a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate;

a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a continuous metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the continuous metallic layer portion such that the non-through holes are electrically connected to each other; and

an IC component having a terminal side including a plurality of terminals, and a non-terminal side which is opposite to the terminal side, the IC component being loaded in the opening of the first substrate such that the non-terminal side of the IC component contacts the metallic layer portion and the terminals of the IC component face outward of the opening in the first substrate,

wherein the IC component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component.

Claim 2 (Canceled)

Claim 3 (Previously Presented): The multi-layer printed wiring board according to claim 1, wherein the external terminals of the first substrate are disposed offset the external terminals of the second substrate.

Claim 4 (Previously Presented): The multi-layer printed wiring board according to claim 1, further comprising a plurality of conductive non-through holes provided in the first substrate and connected to the external terminals of the first substrate and a plurality of conductive non-through holes provided in the second substrate and connected to the external terminals of the second substrate, wherein the conductive non-through holes in the first substrate and the conductive non-through holes in the second substrate are positioned offset from each other.

Claim 5 (Canceled)

Claim 6 (Previously Presented): The multi-layer printed wiring board according to claim 4, wherein the conductive non-through holes in the first and second substrates are provided with a plurality of conductive bumps, respectively.

Claim 7 (Previously Presented): The multi-layer printed wiring board according to claims 1, further comprising a plurality of bonding pads provided for wire bonding the IC component in the first substrate.

Claim 8 (Previously Presented): The multi-layer printed wiring board according to claim 7, wherein the plurality of bonding pads are connected to a plurality of conductive non-through holes formed underneath the plurality of bonding pads, respectively.

Claims 9-10 (Canceled).

Claim 11 (Previously Presented): The multi-layer printed wiring board according to claim 7, wherein the bonding pads have a rectangular shape.

Claim 12 (Previously Presented): The multi-layer printed wiring board according to claim 8, wherein the plurality of conductive non-through holes formed underneath the plurality of bonding pads, respectively, has a plurality of conductive bumps, respectively, on an opposite face of the bonding pads.

Claims 13-17 (Canceled)

Claim 18 (Previously Presented): The multi-layer printed wiring board according to claim 1, wherein the external terminals of the first substrate are positioned in a peripheral form surrounding the IC component, and the external terminals of the second substrate are positioned in a grid form.

Claim 19 (Previously Presented): The multi-layer printed wiring board according to claim 1, wherein the IC component has a bottom portion of which an entire surface of the bottom portion of the IC component is loaded over the metallic layer portion in the second substrate.

Claim 20 (Previously Presented): The multi-layer printed wiring board according to claim 1, wherein the first substrate has a plurality of terminals positioned to be connected to the plurality of terminals of the IC component, and the external terminals and terminals in the first substrate are positioned to face the opposite side of the metallic layer portion of the second substrate.